

Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 1. (currently amended) A television signal receiver, comprising:
2 a first circuit board including a memory and control circuitry for controlling an
3 operation of the receiver, the control circuitry controlling the operation of the receiver in
4 response to data stored in the memory; and
5 a second circuit board operably coupled to the first circuit board via inter-
6 integrated circuit ~~HC~~ bus lines, the second circuit board including a controller, coupled
7 to the inter-integrated circuit ~~HC~~ bus lines, for generating first control signals in
8 accordance with a first signal format in a first operational state and second control
9 signals in accordance with a second signal format in a second operational state,
10 the controller placing the memory into an unpowered state during the second
11 operational state, the memory being coupled to means for preventing the memory from
12 keeping the bus ~~control~~ lines at a low state when the memory is in the unpowered state,
13 wherein the memory and the control circuitry are coupled to the inter-integrated
14 circuit ~~HC~~ bus lines, and the controller transmits the first control signals to the memory
15 via the inter-integrated circuit ~~HC~~ bus lines without affecting the control circuitry in the
16 first operational state, and transmits the second control signals to the control circuitry
17 via the bus ~~control~~ lines without affecting the memory in the second operational state.

1 2. (currently amended) The television signal receiver according to claim 1, further
2 comprising means for preventing the memory from keeping the bus control lines in the
3 low state while the memory is in the unpowered state comprises a zener diode.

1 3. (original) The television signal receiver according to claim 1, wherein the
2 memory includes operational data for controlling deflection circuitry and the control
3 circuitry controls the deflection circuitry in response to the operational data.

1 4. (original) The television signal receiver according to claim 3, wherein the first
2 operational state corresponds to an OFF state of the receiver, and the second
3 operational state corresponds to an ON state of the receiver.

1 5. (currently amended) The television signal receiver according to claim 3,
2 wherein the first control signal corresponds to IIC compliant signals and the second
3 control signals are pulse width modulated PWM signals.

1 6. (currently amended) The television signal receiver according to claim 3,
2 wherein the control circuitry is coupled to the inter-integrated circuit IIC bus lines via
3 bipolar transistors.

1 7. (currently amended) A signal processing apparatus, comprising:
2 a first circuit board including first electronic circuitry, and second electronic
3 circuitry for controlling at least one operation of the receiver; and
4 a second circuit board operably coupled to the first circuit board via control lines,
5 the second circuit board including a controller, coupled to the control lines, for
6 generating first control signals in accordance with a first signal format in a first
7 operational state and second control signals in accordance with a second signal format
8 in a second operational state,

9 the first ~~second~~ electronic circuitry being placed in an unpowered state during the
10 second operational state, the first ~~second~~ electronic circuitry being coupled to means
11 for preventing the first electronic circuitry from keeping the control lines at a low state
12 when the first ~~second~~ electronic circuitry is in the unpowered state, and
13 the first and second electronic circuitry are coupled to the control lines, and the
14 controller transmits the first control signals to the first electronic circuitry via the control
15 lines without affecting the second electronic circuitry in the first operational state, and
16 transmits the second control signals to the second electronic circuitry via the control
17 lines without affecting the first electronic circuitry in the second operational state.

1 8. (original) The signal processing apparatus of claim 7, wherein the first
2 electronic circuitry comprises a memory circuit having operational data stored therein
3 for controlling the second electronic circuitry, the controller retrieving the operational
4 data in the first operational state and controlling the second electronic circuitry in
5 response to the operational data in the second operational state.

1 9. (original) The signal processing apparatus of claim 8, wherein the operational
2 data comprises voltage data for controlling deflection circuitry, and the second
3 electronic circuitry controls the deflection circuitry in response to the voltage data.

1 10. (original) The signal processing apparatus of claim 9, wherein the first
2 operational state corresponds to the apparatus being in an OFF state and the controller
3 and the first electronic circuitry is powered by a standby power supply, and the second
4 operational state corresponds to the apparatus being in the ON state.

1 11. (cancelled)

12. (original) The signal processing apparatus of claim 7, wherein the first control signals comply with the IIC standard and the second control signals comprise pulse width modulated signals.

13. (original) A method of operating a television signal receiver, the method comprising steps of:

providing first and second circuit boards coupled via control lines, the first circuit board having a memory device and control circuitry included thereon and coupled to the control lines, the second circuit board having a controller included thereon and coupled to the control lines;

transmitting via the control lines, first control signals in accordance with a first signal format from the controller on the second circuit board to the memory device on the first circuit board, without affecting the control circuitry, when the receiver is in a first operational state; and

transmitting via the control lines, second control signals in accordance with a second signal format from the controller to the control circuitry on the first circuit board, without affecting the memory device, when the receiver is in a second operational state; and

placing the memory device in an unpowered state during the step of transmitting the second control signals, the memory device being coupled to means for preventing the memory device from keeping the control lines in a low state when the memory device is placed in the unpowered state.

14. (currently amended) The method of claim 13 44, wherein the first operational state corresponds to the receiver being in the OFF state wherein the controller and the

3 memory device is supplied by a standby power supply, and the second operational
4 state corresponds to the receiver being in an ON state.

1 15. (currently amended) The method of claim 13 ~~15~~, wherein the first control
2 signals enable the controller to read data from the memory device.

1 16. (currently amended) The method of claim 13 ~~16~~, further comprising the step
2 of controlling deflection circuitry via the control circuitry in response to data read from
3 the memory device.

1 17. (currently amended) The method of claim 13 ~~14~~, wherein the first transmitting
2 step comprises transmitting the first control signals in accordance with the IIC standard.

1 18. (currently amended) The method of claim 13 ~~14~~, wherein the second
2 transmitting step comprises transmitting the second control signals as pulse width
3 modulated PWM signals.

1 19. (currently amended) The method of claim 13 ~~14~~, wherein the providing step
2 comprises providing the first circuit board having the control circuitry ~~circuit~~ coupled to
3 the control lines via bipolar transistors.